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PATENT APPLICATION

Inspection System and Semiconductor Device Manufacturing Method

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Title of the Invention

INSPECTION SYSTEM AND SEMICONDUCTOR DEVICE MANUFACTURING METHOD

Field of the Invention

The present invention relates to inspection systems in the manufacture of electronic devices such as semiconductor integrated circuits and also to methodology for manufacturing electronic devices using the same.

Background of the Invention

In the manufacture of electronic devices typically including semiconductor integrated circuits, after detection of defects using dark-field wafer inspection apparatus and/or bright-field wafer inspection apparatus, image taking apparatus with a built-in electron microscope or else, for example review apparatus, is used in some cases for the purpose of analyzing the individual defects thus detected. It should be noted that while the dark-field wafer inspection apparatus is the one that is operable to detect particles attached to wafers whereas the bright field wafer inspection apparatus is for detection of pattern defects as formed on wafers, such particles and pattern defects will be generally called the "defects" in following description.

Presently available review apparatus is generally

designed to sense or pick up the position of an individual defect as an image of higher resolution than dark-field wafer inspection apparatus and bright-field wafer inspection apparatus. Due to this, the review apparatus is not for image pickup of the positions of all possible defects as detected by inspection apparatus but for execution of sampling of defect positions within wafer surfaces and for performance of an image sensing operation with respect to several limited portions only. Traditionally this sampling has been achieved by execution of random sampling-that is, random selection of defects from among those defects detected.

In addition, as disclosed in Published Unexamined Japanese Patent Application No. 10-214866 ("JP-A-10-214866"), there is a technique for classifying, in cases where cluster-shaped defects such as scars and clustered defects or the like are present, those defects as detected by inspection apparatus into ones inside of the cluster-like defects and the others outside thereof; however, even in this case also, random sampling of several portions from the inside of such cluster-like defects was done while randomly sampling several other portions from the outside.

With the prior art random sampling technique, although it is possible to statistically recognize the tendency of defects, this is incapable of ensuring achievement of efficient reviewing of any required defects-for example, it is impossible

to provide any priority-added remedy for critical defects that can lead to occurrence of unwanted electrical failures, which in turn makes it difficult to effectively improve the resultant yield of production.

Summary of the Invention

It is therefore a primary aim of the present invention to provide an inspection system capable of improving the inspection efficiency through judgment of certain defects to be reviewed with higher priority. Another aim is to improve thereby the manufacturing yield of semiconductor devices.

We have taken into careful consideration the relationship of a defect distribution and LSI chip layout, and then proposes a specific technique for enabling selection of defects to be reviewed with higher priority.

Fig. 10 is a diagram showing a distribution of defects within the chip to be detected by the inspection apparatus.

This diagram is the one that dots data 35 of defects detected by the inspection apparatus into a schematic diagram 32 of the design circuit layout of an LSI chip. More specifically, it is the one that adds as points such detected defects by use of position coordinates within each LSI chip on a wafer. Black-painted circles represent the individual defects. Rectangular frames of from B1 to B7 are the positions of an LSI blocks 1 to LSI block 7, respectively. Here, the term

"LSI block" as used herein refers to an A/D converter block, D/A converter block, memory block, processor block or the like in the case of mobile wireless telephone handsets, by way of example. LSI blocks are generally called the circuit blocks, which have independent functions within an LSI and layout of which is also separated except for electrical connection of circuits used therein.

As apparent from viewing the same diagram, a distribution of defects detected by the inspection apparatus is closely related to the circuit layout, and exhibits the tendency which follows.

(1) Defect density is different depending upon the circuit pattern density of circuit layout. In a region in which the circuit layout is coarse and rough, a greater number of defects will be detected at inspection apparatus than in dense regions. Generally, the coarse density of circuit pattern differs in units of LSI blocks; for example, processor blocks are less in circuit pattern width than memory blocks and yet greater in layout density than the latter. Hence, an increased number of defects are to be detected in processor blocks than in memory blocks.

(2) At LSI block edge portions (contour parts) of the circuit layout, a great number of defects are detected. In many cases, this is due to the fact that the inspection apparatus erroneously detects those objects which are actually not defects

as defects. These detection errors occur at specific portions with greater convex-concave differences of circuit patterns by using the inspection apparatus. Here, the term "edge portion (contour part)" is used to mean a boundary between circuit blocks associated therewith, which boundary has widths ranging from several tens to several hundreds of micrometer.

Thus, it has been affirmed that upon selection through simple random sampling of defects to be reviewed, the next problem occurs, resulting in incapability to efficiently perform sampling of such to-be-reviewed defects, e.g. those defects which can become electrical failures with higher probabilities.

In view of the above, the present invention attains the foregoing objects by employing its unique technique for selecting such to-be-reviewed defects by use of LSI's design layout. More specifically, LSI design layout information is used to review certain defects that are not in close proximity to LSI block contour portions with higher priority or alternatively to review those defects being present in LSI blocks of dense circuit pattern widths with higher priority.

Additionally a technique is used for obtaining failure probability (kill ratio) relative to defect size in units of LSI blocks and for reviewing defects high in this failure probability. Whereby, specified defects high in possibility to give influence to production yield will first be reviewed

efficiently, which in turn makes it easier to inquire and clarify several factors with direct influenceability within a shortened time period, thus shortening a time as made failure products and improving the manufacturing yield. In particular, with a specific type of products with a variety of circuit blocks being present in a single LSI, such as the so-called system LSIs, judging defects to be reviewed with higher priority is important for yields improvements at earlier stages in the manufacture thereof.

Brief Description of the Drawings

Fig. 1 is a diagram showing one example of the procedure of processing applied to selection of a defect or defects to be reviewed.

Fig. 2 is one example of a block diagram showing an arrangement of hardware.

Fig. 3 is one example of defect map data.

Fig. 4 is one example of two-dimensional (2D) map data of Fig. 3.

Fig. 5 is an enlarged diagram of a chip row 1 and chip column 1 of Fig. 4.

Fig. 6 is an example of circuit layout data.

Fig. 7 is an example of a method for calculation of failure probability data.

Fig. 8 is an example of an ensemble of failure probability

data.

Fig. 9 is an example of a file of layout data.

Fig. 10 is an example of a relation diagram of a distribution of defects within a chip versus circuit layout.

Fig. 11 is an example of failure possibility-added defect map data.

Fig. 12 is an example of failure possibility-added defect map data as aligned based on failure possibility.

Fig. 13 is one exemplary to-be-reviewed defect selection result.

Fig. 14 is another exemplary to-be-reviewed defect selection result.

Fig. 15 is still another exemplary to-be-reviewed defect selection result.

Fig. 16 is an example of a review condition file.

Fig. 17 is an example of a block diagram showing a structure of circuit layout.

Fig. 18 is an exemplary on-screen display image of an inspection system.

Fig. 19 is another exemplary on-screen display image of the inspection system.

Description of the Preferred Embodiment

One preferred form of the present invention will now be set forth in detail with reference to the accompanying

drawings below.

Fig. 2 is a block diagram showing one example of a system configuration of the present invention.

Reference numeral "51" is used herein to designate an inspection apparatus; 52 denotes a review apparatus; 53 is a layout CAD apparatus. Numeral 60 designates a analysis unit, which is a computer system having an arithmetic processor unit 61, main storage device 62, auxiliary storage device 63, user interface 64, and network interface 65. The inspection apparatus 51 , review apparatus 52, layout CAD apparatus 53 and analysis unit 60 are operatively connected and linked together via a local area network 54 for permitting data transmission thereamong where necessary.

The inspection apparatus 51 may be a dark field wafer inspection apparatus or a bright field wafer inspection apparatus operable to output information as to coordinate positions and sizes of defects within wafer surfaces. Defect map data that is an inspection result of the inspection apparatus 51 is stored in test database of the auxiliary storage device 63 via the local area network 54 and the network interface 65 and the main storage device 62 of analysis unit 60, along with data items indicative of product type names, lot numbers, wafer numbers, layer names and others. Fig. 3 shows one example of the defect map data as detected at the inspection apparatus. Defect map data 21 has information concerning the coordinate

positions and sizes within wafer surfaces in units of defects. In the illustrative embodiment, the defect map data 21 involves a defect number, chip column, chip row, X- and Y-coordinates and defect diameter as written thereinto on a per-defect basis. The defect number is a through number which is added to a defect as detected at the test apparatus. The chip column, chip row and X- and Y-coordinates are for indication of a defect coordinate position. The chip column and chip row indicate the position a chip within a water and the X- and Y-coordinates indicate the position of a defect within a chip. To be brief, these are for description of the states shown in Figs. 4 and 5. Fig. 4 is the one that pictorially depicts the defect map data 21 of Fig. 3 as a two-dimensional (2D) map. A circle 22 represents a wafer; rectangular frames inside of 22 indicate chips respectively. The chip column and chip row of the defect map data 21 indicate chip arrays from a wafer edge. Black plotted points of from 101 to 110 are positions of detects with the defect numbers of 21 of from 1 to 10 based on the chip column and chip row and X- and Y-coordinates. Fig. 5 is an enlarged chip belonging to the chip column 1 and chip row 1 of Fig. 4. A rectangular frame of 31 denotes a chip, wherein the one with the position of a defect number 1 plotted based on the X- and Y-coordinates of 21 with a lower left edge being as an origin is 101.

On the other hand, circuit layout data with design

completed at the layout CAD apparatus 53 is stored in the auxiliary storage device 63 along with a product type name and layer name via the local area network 54 and network interface 65 and main storage device 62 of analysis unit 60. One example is that position information of blocks B1-B7 in a chip is generated from the circuit layout data and is stored as layout data in the auxiliary storage device 63. Note that this layout data should not exclusively be generated from the layout CAD apparatus and may be merely stored in auxiliary storage device 63 along with the product type name and layer name.

Fig. 9 shows one example of the layout data. With a layout data file 72 shown in Fig. 9, the position information of an LSI block m1 is stored together with a product type name LOGIC 234, layer name METAL1 and failure probability data of block name m1, wherein the coordinates thereof refer to a rectangle with X=5, Y=80 and X=20, Y=95 within the chip being diagonal vertex coordinates. Additionally in this file, the relation of each defect diameter versus failure probability is described. This layout data file is formed per each of the LSI blocks B1-B7 shown in Fig. 10.

Here, an explanation is given of one example of the method for calculating the failure probability by use of the circuit layout data in accordance with a defect diameter.

Fig. 6 is one example of the circuit layout data. The circuit layout data are 2D graphics data of mask patterns

for use during transfer of a circuit pattern at photolithographic apparatus of an LSI. 32 is a schematical diagram of a circuit layout, wherein rectangular frames of from B1 to B7 are positions of an LSI block 1 to LSI block 7 respectively. An enlarged view of part within B6 (portion indicated by oblique lines within rectangular frame) is 33. White portions of 33 are circuit pattern-less portions whereas gray portions are the circuit pattern.

Fig. 7 is a diagram showing a method for calculating failure probability (kill ratio) data from the circuit layout data. This method is presently applied to yield prediction schemes as disclosed in Published Unexamined Japanese Patent Application Nos. 48-40376 and 8-162510 and also in C. H. Stapper, "Modeling of Defects in Integrated Circuit Photolithographic patterns," IBM Journal of Research and Development, Vol. 28, No. 4, 1984. More specifically, the so-called Monte Carlo simulation is applied to the circuit pattern of each layer of the circuit layout data, thereby causing virtual circular defects of the same diameter to generate at random positions. 34 is an enlarged view with the circuit patterns being collated with such virtual defects. In this example, virtual defects with oblique lines added to circular frames of 121, 122 become electrical short circuit failures; in contrast, virtual defects indicated by white-painted circles of from 123 to 129 will not result in any electrical failures.

The failure probability at this part is two-ninths, wherein those plotted with the vertical axis being as the failure probability and with transverse axis as defect diameter are white-pained rhombic plot points. Such simulation is performed for various virtual defects with different diameter values, thus plotting white-pained triangles. A curve passing though the triangular plot points and rhombic plots is a failure probability data curve 71. Fig. 8 is a diagram showing pictorial representation of an ensemble or "assembly" of failure probability data items. This is the one wherein the simulation shown in Fig. 7 is performed with respect to each product type and each layer on a per-LSI block, on a per-entire chip surface or on a per-2D region basis, thereby to calculate failure probability data respectively. And, based on this, the layout data file 72 shown in Fig. 9 is to be obtained in units of respective LSI blocks.

The auxiliary storage device 63 also stores therein review conditions used for selection of defects to be reviewed as will be described later and programs until selection of more than one to-be-reviewed defect to be later described.

An explanation will next be given of a flow of a series of processing tasks for selection of more than a to-be-reviewed defect with reference to Fig. 1.

Firstly, when a wafer that has passed the inspection at the inspection apparatus 51 is set at the review apparatus

52, wafer ID is read at review apparatus 52 (at step 101). Additionally its layer name is set up.

Upon inputting of the wafer ID and layer name, these information items are sent to the main storage device 62 of the analysis unit 60 through the local area network 54 and network interface 65. Note here that the wafer ID is the information indicative of a product type name, lot number and wafer number.

Step 102 searches any corresponding defect map data (see Fig.3) to be stored in the auxiliary storage device 63 based on the received information of wafer ID and layer name, and then stores such searched defect map data into the main storage device 62.

Step 103 reads an ensemble of layout data 72 (see Fig. 9) within the auxiliary storage device 63 based on the wafer ID and layer name being stored in the main storage device 62, and stores it in the main storage device 62.

Next, step 104 calculates the number of defects of the defect map data as stored in the main storage device 62 at step 102, and thereafter step 105 executes the following processing, with respect to a respective one of defect numbers 1 to "N".

For each defect of the defect map data, step 106 compares such defect's X- and Y-coordinates to layout data block coordinates to determine or "judge" a block name to which

the defect belongs while at the same time judging whether such defect's position is a block edge or not and then stores the judgment result in the main storage device 62. Here, whether the defect is in a block edge or not may be determined in such a way that if a distance from the defect to an LSI block edge is less than a predesignated threshold value then such defect is determined to be present at the block edge. An alternative approach is to represent the distance by coordinates indicative of an allowable range and then make a decision by determining whether it falls within the coordinate range. As the defect's position coordinates are set by chip coordinates rather than wafer coordinates in this embodiment, it is possible to readily perform comparison with the above-noted layout data block coordinates with respect to all the chips concerned. In case more than one types of LSIs are formed in a single wafer, comparison may be done while setting the layout data for each LSI.

Next, Step 107 calculates a failure probability to be defined in its corresponding layout data 72 based on the defect map data's defect diameter being stored in the main storage device 62, then, stores the calculation result in the main storage device 62.

Next, step 108 reads the block name, data indicating whether block edge or not , and the failure probability which have been calculated at the steps 106-108 and stored in the

main storage device 62, then generates failure probability-added defect map data. Fig. 11 is an example of such failure probability-added defect map data. The failure probability-added defect map data 23 is such that results of obtaining the belonging LSI block, whether LSI block or not, and the failure probability are added to the defect map data 21 shown in Fig. 3. Step 109 Repeats these processings with respect to all available defects.

Next, Step 110 reads a review condition file within the auxiliary storage device 63 based on the wafer ID and layer name stored in the main storage device 62 and then stores it in the main storage device 62 (step 110). Here, the review condition is the one that may be freely set by users, for example, a certain condition for extraction of only defects with the failure probability being greater than or equal to a prespecified value, condition for extraction of those defects that are not present at block edges, condition for extraction of only defects with defect sizes greater than or equal to a preselected value or alternatively less than or equal thereto, condition for extraction of only defects being present in specified blocks, or condition for extraction of a predetermined number of ones from each block. Alternatively, there is also employable a condition for combination of some or all of these. A merit of these schemes is that those defects which can cause electrical failures may be efficiently selected from among

an increased number of defects as detected at the inspection apparatus. A practically meaningful review condition is to select specific defects with influenceability to production yield while excluding defects with no influence upon the yield.

Fig. 16 is an example of the review condition file. 41 is an example of the file that is stored in the auxiliary storage device 63 while permitting a person in charge of defect analysis to establish an appropriate review condition from the user interface 64 of the analysis unit 60. In this example, a review of a product type name LOGIC 234 and layer name METAL1 is capable of letting maximally twenty defects be the to-be-reviewed objects and, simultaneously, an instruction is made to review defects excluding those being present at block edges of LSI blocks B1, B2 except for certain defects which have the failure probability greater than or equal to 0.30 and also belong to an LSI block B5. Thus specific defects of those detected at the inspection apparatus 51 which satisfy this condition will be reviewed at the review apparatus 52.

Next, step 111 sorts the failure probability-added defect map data 23 within the main storage device 62 in serial order so that data with higher failure probability comes before the others, and then stores in the main storage device 62. Fig. 12 is defect map data 24 sorted based on failure probability. This is the one that lets the failure probability-added defect map data 23 of Fig. 11 be recorded so that one with higher

failure probability comes before the others. Note here that if review is done without regard to the failure probability then, obviously, this step-and further, the step of calculating the failure probability-and any associative arrangements thereof will no longer be required. However, in view of the fact that the failure probability is also a parameter or "barometer" that clearly indicates critical defects, it can be said that reviewing such defect with higher failure probability is effective for reviewing certain defects with the highest criticality.

Next, step 112 classifies defect map data into the defects of interest and the defects of no interest under the review condition within the main storage device 62, then selects one or more defects to be reviewed, and then stores then in the main storage device 62.

Fig. 13 is an example of such to-be-reviewed defects as selected from the defect map data 23. 26 is an example with the upper five defects-these are selected from the defect map data 23 as has been sorted based on the failure probability while excluding those defects judged to be present at LSI block edges-being specified as the to-be-reviewed defects. A merit is that any defects as detected from LSI block edges, which are high in possibility of being non-criticality, are capable of being excluded successfully.

Fig. 14 is another example of selection of to-be-reviewed

defects from defect map data 24. 27 is an example with the upper five defects being specified as the to-be-reviewed objects, wherein the five defects are selected from the defect map data 24 as has been sorted based on the failure probability while excluding those defects belonging to an LSI block m5. A merit is that any defects as generated at m5, which are known in advance based on the experience not to be critical, are capable of being excluded successfully.

Fig. 15 is still another example of selection of to-be-reviewed defects from the defect map data 23. 25 is an example with the upper five defects of the defect map data 24 as sorted based on the failure probability being specified as the to-be-reviewed defects. Exactly how many upper-level defects are specified as the to-be-reviewed defects is determinable depending upon the actual processing rate of the review apparatus and/or LSI wafer production volume or the like. In this case also, since the failure probability being calculated is changed in value in accordance with the layout, i.e. the dense-and-coarse degree of each block, it becomes possible for those defects with a tendency to become critical defects to be reviewed in accordance with the layout.

Lastly, step 113 transfers the to-be-reviewed defect selection result within the main storage device 62 to the review apparatus 52 via the network interface 65 and local area network 54. The review apparatus 52 performs a reviewing

operation from a defect with higher priority order based on the to-be-reviewed defect selection result thus received. At this time the coordinates of such defects have already been defined in this to-be-reviewed defect selection result; thus, it is possible to drive the review apparatus 52 based on this information. Also note that if defects to be reviewed are selected due to the to-be-reviewed defect selection result then a technique is employable for again selecting the order of to-be-reviewed defects therein in order to review efficiently. This may be executed at either one of the review apparatus 52 and the analysis unit 60.

Fig. 17 is a diagram showing one example of the structure of circuit layout data. Circuit layout data of a single LSI is generally designed to have a hierarchical structure in units of LSI blocks as shown in the same drawing. A "root" is to be understood to mean an entire LSI, wherein B1 to B7 are LSI blocks. Furthermore, B11, B12, B21, B22, B41, B51, B52, B53, B61, B62, B121, B221, B531, B532 and B5321 are sub-blocks of LSI blocks or, alternatively, further subblocks of subblocks. In this example, LSI blocks of from B1 to B7 are included in the root. In addition, subblocks of B11 and B12 are involved in LSI blocks B1. Further, B121 is included as a subblock of B12. Here, the LSI block's hierarchical structure is hierarchical in functionality and, thus, does not mean any layer of the LSI. Several layers are present

in the same block and subblock. Additionally the same layer's circuit pattern is included in different blocks. Due to this, the simulation for obtaining the failure probability as has been explained in conjunction with Fig. 7 is done in a way such that a circuit pattern of the same layer is extracted from each block of this structure to thereby prepare per-layer data.

Fig. 18 is an example of an on-screen display image of the analysis unit 60. This drawing is the one that shows defect map data of a layer name METAL1 with a product type name LOGIC 234, lot number LOT55 and wafer number 10. Here, this is a result obtained after having selected to-be-reviewed defects while applying thereto the review condition 41 shown in Fig. 9. 81 is the one that displays a defect position distribution with such defect map data being dotted using the coordinates within a chip, which provides a display while referencing a schematic diagram of circuit layout. 82 is the one that displays defect map data at a wafer level. Both of them are the ones that display the same defect map data. Black triangles are results of selection as to-be-reviewed defects. Here, there are three defects satisfying the review condition 41. White-painted circles are defects as determined under the review condition 41 to be excluded from the to-be-reviewed defects irrespective of the failure probability thereof whereas black circles are defects which have failed to become any

to-be-reviewed defects due to the fact that their failure probability are less than 0.30. In this way, simultaneously displaying the defects as selected as to-be-reviewed defects along with on-chip defect distribution and/or circuit layout as well as the wafer level makes it possible to recognize any to-be-reviewed defects with increased understandability. Here, when displaying the schematic diagram of circuit layout such as 81, the detailed circuit layout as has been explained in Fig. 17 no longer is required. Then, in order to rapidly display the entirety of a chip of the circuit layout data, it is effective to compress such circuit layout data in the auxiliary storage device 63 as bitmap data.

Fig. 19 is another example of the on-screen display image of the analysis unit 60. This drawing is the one shows the same defect map data as that of Fig. 18, which is a result of selection of to-be-reviewed defects with the review condition 41 applied thereto. 81 is the same as that of Fig. 18. 83 is a result obtained through a process having the steps of clicking while letting a cursor 84 be pointed at a single defect within 81 and at this time searching and visually displaying the layout data of circuitry near or around it. At 83, a circular frame 85 is drawn with the position of such defect being as the center in a way pursuant to the size of the defect, thereby enabling easy recognition of the relation of this defect versus circuit pattern prior to execution of

reviewing. In addition, 86 is a graph pictorially depicting a failure probability data curve of an LSI block in which the defect clicked with the cursor 84 is present; 87 is the size of such defect clicked. In this way, visually displaying both the defect size and the failure probability data at a time makes it possible to confirm the reason why it is selected as this review defect. Here, the review condition is to be determined by selection of review-unnecessary circuit blocks or selection of block edges or alternatively definition of failure probability, based on a result obtained after execution of reviewing without any inspections and conditions.

So far, the same layout data file (Fig. 9) is used without regard to on-wafer chip positions; however, the rate of occurrence of critical defects can differ within wafer surfaces in many cases. In particular, the quest for larger wafer diameters makes such phenomenon more appreciable. For the purpose of cope with this phenomenon, one exemplary approach is to perform defect selection by employing in combination prior known random sampling techniques and the above-discussed method for selecting defects with the failure probability. In other words, both the process of reviewing defects through prior art random sampling and the above-stated process of reviewing by using the failure probability-based defect selection methodology are performed at a time. This also makes it possible to uniformly select on-wafer defects.

Alternatively, similar effects are obtainable either by extracting them through random sampling from among failure probability results greater than or equal to a prespecified value or by performing random sampling from among those defects absent at any block edges. Still alternative approach is to subdivide an entire wafer surface into certain areas by use of chip coordinates, each of which areas thus divided are then subject to defect extraction. In this case, it would readily occur to those skilled in the art that the finer the areas, the more uniform the review of such entire wafer face.

It has been stated that more efficient inspection than the prior art is achievable by using a specific method during inspection of particles and pattern defects of wafers forming electronic devices, which method includes the steps of sampling certain defects with higher possibility to create electrical failures and then reviewing such defects with higher priority. Similarly, it is also possible to review the defects high in possibility to become electrical failures.

In accordance with the present invention, the use of layout information makes it possible to improve the inspection efficiency by judgment of defects to be reviewed with higher priority. Whereby the resulting yield of production will improve accordingly.